WHAT IS CLAIMED IS:

1. A keeper circuit for a dynamic node of a circuit, wherein the effective strength of the keeper circuit operating on the dynamic node is reduced during an interval in which at least one path in an evaluation circuit is sensitive to a keeper device.

2. The circuit, as recited in claim 1, wherein the sensitivity of the at least one path includes output of an incorrect value of the evaluation circuit output.

3. The circuit, as recited in claim 1, wherein a response to the sensitivity is otherwise a reduced speed of the evaluation circuit output.

4. The circuit, as recited in claim 1, wherein the operation of the keeper circuit on the dynamic node is effectively disabled during the interval.

5. A circuit comprising:

a dynamic node;

an evaluation circuit coupled to the dynamic node; and

a keeper circuit coupled to the dynamic node, wherein the effective strength of the keeper circuit operating on the dynamic node is reduced during an interval in which at least one path in the evaluation circuit is sensitive to a first keeper device.

6. The circuit, as recited in claim 5, wherein the keeper circuit latches an output of the circuit.

7. The circuit, as recited in claim 5, wherein the keeper circuit includes the first keeper device.

8. The circuit, as recited in claim 7, wherein the keeper circuit includes a keeper gating device coupled to the keeper device.

9. The circuit, as recited in claim 5, wherein the keeper circuit includes a weak keeper device.

10. The circuit, as recited in claim 5, wherein the keeper circuit is responsive to a keeper control.

11. The circuit, as recited in claim 10, wherein the keeper control is clocked.

12. The circuit, as recited in claim 10, wherein the keeper control is self-timed.

13. The circuit, as recited in claim 5, further comprising a precharge device.

14. The circuit, as recited in claim 13, wherein the precharge device and the evaluation circuit operate during different phases of a control signal.

15. The circuit, as recited in claim 5, wherein the first keeper device is sized to sufficiently overcome the leakage current in the evaluation circuit.

16. The circuit, as recited in claim 5, wherein the reduction in the effective strength of the keeper circuit occurs before arrival of a fastest signal coupled to a sensitive output path of the evaluation circuit.

17. The circuit, as recited in claim 5, wherein the effective keeper circuit strength is restored after arrival of a slowest signal coupled to a sensitive output path of the evaluation circuit.

18. The circuit, as recited in claim 9, wherein the weak keeper device is minimally sized to sufficiently overcome noise while the first keeper device is effectively disabled.

19. The circuit, as recited in claim 5, wherein the dynamic node is precharged high.

20. The circuit, as recited in claim 19, wherein the evaluation circuit is n-logic.

21. The circuit, as recited in claim 5, wherein the dynamic node is precharged low.

22. The circuit, as recited in claim 21, wherein the evaluation circuit is p-logic.

23. A method for evaluating a dynamic node, comprising:

precharging a dynamic node;

effectively disabling a keeper device coupled to the dynamic node during an interval in which at least one path in an evaluation circuit is sensitive to a keeper device;

evaluating an evaluation circuit; and

effectively enabling the keeper device.

24. The method, as recited in claim 23, further comprising:

protecting the dynamic node from noise during the effective disablement of the keeper device.

25. A method for weakening a keeper circuit, comprising:

reducing effective keeper circuit strength during an interval in which at least one path of an evaluation circuit is sensitive to a strong keeper device.

26. The method, as recited in claim 25 for weakening a keeper circuit, further comprising:

maintaining a weak keeper device during the interval.

27. An apparatus for evaluating a dynamic node, comprising:

means for precharging a dynamic node;

means for effectively disabling a first keeper device coupled to the dynamic node during an interval in which at least one path in an evaluation circuit is sensitive to a keeper device;

means for evaluating an evaluation circuit; and

means for effectively enabling the first keeper device.

28. The apparatus, as recited in claim 27, further comprising:

means for protecting the dynamic node from noise during the effective disablement of the first keeper device.